Lessons Learned in the Implementation of Aerosol Jet Printing for Fabricating Multilayer Circuit Boards

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Additive manufacturing applied to electronics is rapidly growing in volume and revenue worldwide with projections of significant technological impact and market influence in the coming decades[1-5]. Impact areas range from healthcare to energy management to electronic wireless systems[2]. Given that electronics are fundamentally multi-material systems, the challenge lies not just in material formulation but also material-material interaction including chemical compatibility, adhesion, temperature processing, and induced stresses. While initial deposition and functionality of the devices receive the most attention, long term aging and environmental performance are relatively unexplored topics in printed electronics, yet critical for adoption of the technology into field-able systems.

In particular, Internet of Things (IoT) applications require small, conformal modules integrating standard commercial off the shelf (COTS) components with a fast time-to-market and simple circuit customization/revision. This is congruent with additive manufacturing and, in particular, aerosol jet printing (AJP) technology, where the entire system can be deposited on a 3-D, potentially flexible, substrate, and not confined to two-dimensional planes. Other approaches often employ hybrid techniques such as stereolithography (SLA), fused deposition modeling (FDM) and inkjet in conjunction with conductor embedding and pick-and-place tools[5-7]. These methods generally employ multiple tools for different materials at different stages of the manufacturing process.

AJP can deposit both conductors and insulators while maintaining a millimeter-scale standoff distance above the printed surface. This enables conformal printing to 3-D substrates and expands circuit integration to geometries not suited for planar circuits. In addition, this approach shortens the circuit layout and fabrication cycle time to more quickly iterate a given design[1] and reduce material waste[8], particularly hazardous waste, compared to a conventional printed circuit board.

One IoT-relevant example is a Bluetooth transceiver system that integrates a low cost system on chip (SoC) with functional sensing, actuation of LEDs, and RF transmission. This builds on AJP work shown with COTS integration previously[9-11] and emphasizes the multilayer, RF challenges of these systems.

The Nordic Semiconductor nRF51822 Multiprotocol Bluetooth low energy/2.4 GHz RF SoC is an ideal candidate for the IoT demonstration. A transceiver circuit reference design is available, leveraging the COTS demonstration board nRF51 Development Kit (PCA10028), to compare "standard" PCB embodiment with the printed approach, particularly related to line resistivity, power

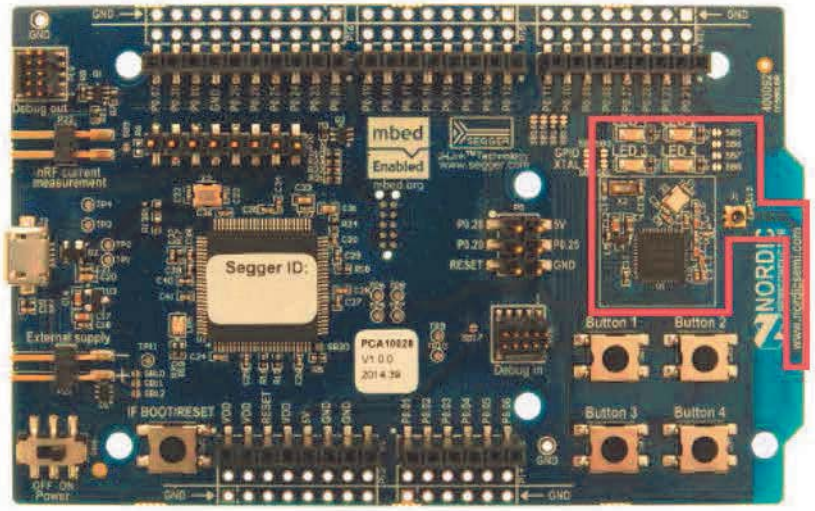

Figure 1: The Nordic Semiconductor nRF51822 Multiprotocol Bluetooth low energy/2.4 GHz RF SoC is shown. The region in red is being relicated with AJP technology.

consumption, and RF performance. The PCA10028 is reprogrammable, has both active and passive components, has an appropriately sized footprint for printing, and uses a variety of easily obtained commercial components so the application scope remains broad, particularly for IoT. Figure 1 shows the full commercial board along with the red region which is being replicated in the AJP circuit. Unnecessary peripherals are stripped out of the design so that the focus is only on interconnection to the chip, power and wireless communication.

Design changes to the original layout make the board more printable. These include reducing the ground plane area, placing the processor in QFN48 package upside down on the board, printing up the sidewall of the processor, and printing over the ground plane on the backside of the chip. This "chips first" approach builds up the electrical interconnect around the SoC. This relaxes the alignment restrictions on part placement and circumvents standard attach methods which can dissolve the AJP ink. Finally, the additive approach to dielectric deposition changes the layout rules versus standard subtractive PCB layouts that remove dielectric to create vias.

NovaCentrix HPS-030AE1 Silver Flake Ink and Corin XLS polyimide ink served as the AJP conductor and dielectric, respectively. The SoC was affixed to the substrate with Armstrong C-7/W epoxy (C-7) and other components conductively attached with Epotek H20E for prototyping and proof of concept. They could also be integrated first along with the SoC.

Fabrication starts with placing the microprocessor (QFN48 package) upside down and attaching to the substrate with C-7. Enough C-7 is used during this attach to make an epoxy fillet along the edge of the microprocessor package. This eliminates the airgap between the package and the substrate which can prove difficult to bridge with conductive inks.

Conductive traces integrating the package to the circuit are then printed with silver ink up the package sidewall. Five passes are used in order to thicken the trace and reduce the resistance. This approximately correlates to a thickness of 3-4 µm. Figure 2 highlights the flipped QFN package and the sidewall interconnect.

The ground plane is printed immediately after the sidewall integration traces on the QFN48 package. This is done without sintering of the sidewall traces to reduce heat exposure to the QFN48 package. Two passes are done in order to build up the thickness of the ground plane and reduce resistance. This correlates to a thickness of around 2 µm.

After the sintering of the ground and interconnect layers, which is done at 250°C for one hour, the dielectric layer is printed in patches. Dielectric is only dispensed in areas of need. For most areas, as long as the dielectric provides electrical insulation, the thickness doesn't matter. Generally the dielectric is built up with three passes of polyimide. However, the thickness is of critical importance for the RF circuitry, as discussed later. The polyimide is cured at 200°C for one hour.

The upper conducting layer is printed last. This layer includes pads for components down to a 0201 footprint (imperial units) in the RF portion of the circuit. Figure 3 shows two different locations on the board with a multilayer scheme. After this layer is sintered at 200°C for 1 hour, the board is populated with the rest of the parts and attached with conductive epoxy. Figure 4 shows the

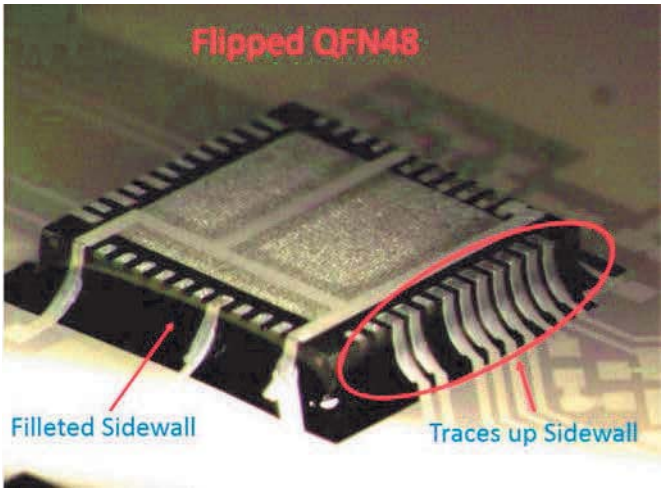

Figure 2: The flipped microprocessor (QFN48 package) with printed interconnect is shown. The glue fillet provides a ramp for the printed ink to traverse the sidewall of the package and make the pad to routing connections. On top of the package there are routing traces connecting pads together. They are shielded from the package ground plane by polyimide.

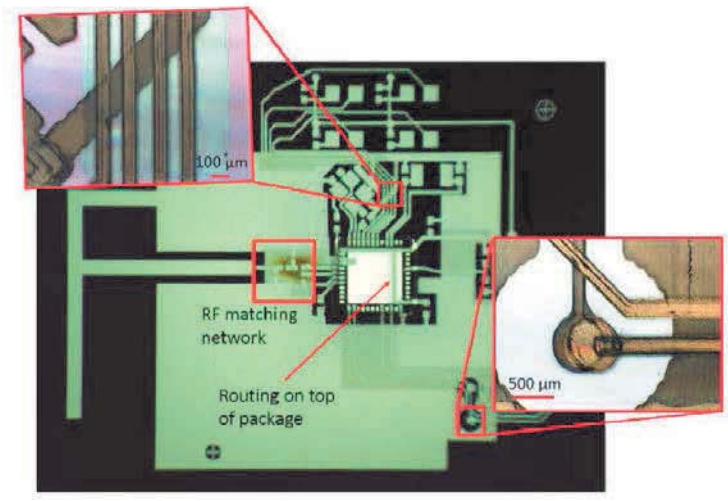

Figure 3: The transceiver circuit after printing of the routing layer is shown. Two locations are called out which show a multilayer stack up of conductor-dielectric-conductor. The targeted deposition of the dielectric is fundamentally different than traditionally PCB manufacture which removes dielectric from select areas.

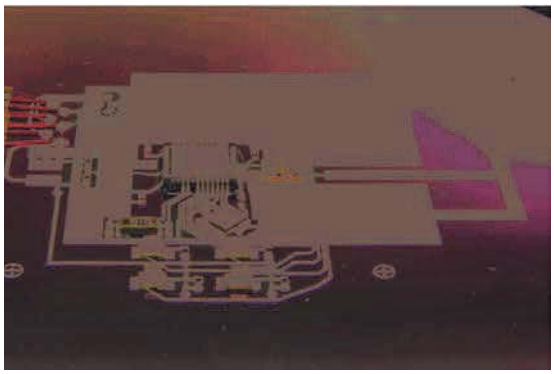

Figure 4: The final board after it was populated with COTS components is shown.

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completed transceiver circuit. Printed lines were designed to 25 micron width and 2-5 micron height. While material output variation, ink properties, and the aerosol jet stream can cause more geometric variation compared to PCB technology, misprints can be corrected with a simple isopropyl alcohol wash and reprint prior to ink cure.

This IoT platform provides a quantitative measure of fabrication time reduction and rapid design iteration. After the preliminary design, significant and sequential changes, particularly the dielectric patterning, each took no more than an hour, including machine code generation. The fabrication time was reduced to 10 hours and there is potential to reduce it by approximately 4 more hours by changing the sintering/annealing process and employing an automated tool for population of the circuit board components. Other approaches to sintering such as photonic annealing could reduce cure time from hours to seconds per layer.

The SoC is programmable via attached SPI port wires, resulting in successful boot of the system which executed a program that blinks three LEDs in a pattern. The traces have a resistivity 3-7x higher than that of PCB copper and result in nearly the same increase in total power consumed since trace loss dominates total power for this low-power design. The acceptability of this resistivity difference is largely application dependent. Silver traces reaching nearly 50% of the conductivity of bulk silver have been reported elsewhere, so further process improvement may be possible as well.

The RF portion of the circuit is most challenging due to the inconsistency of the microstrip antenna dielectric. Design and modeling calls for a 10 micron thick dielectric; a +/- 3 micron difference would lead to RF failure. Process variations and conditions in dielectric deposition did not yield this tolerance, therefore the Bluetooth communication portion of the system is nonfunctional. This highlights a critical future direction for development of AJP system electronics – new dielectric inks and processes to achieve uniform dielectric layers for multilayer RF antennas.

Overall yield of the limited number of circuits printed and assembled was less than 30%. The primary failure mechanisms are electrical shorting from layer-to-layer misalignment and conductive epoxy bridging electrical layers due to chemical incompatibility. The first can be solved with improved fiducial locations and alignment procedures. The second can be resolved by material change or component attach with AJP to preclude the need for epoxy.

Finally, environmental and aging testing employed typical test structures to assess the long term viability of the ink/dielectric system. First, a thermal shock test was conducted according to IPC-TM-650-2.6.7.2a Thermal Shock. The test units were exposed to temperatures of -55˚C to 125˚C in 15 minute cycles for 1000 cycles. Then, a moisture and insulation resistance test was conducted at 50°C/85% relative humidity regime according to IPC-TM-650-2.6.3F. This test was conducted for 5 days. Last, some structures were put into an oven at 60°C for months to determine the effect of lab humidity and elevated temperature on the structures. This was not done to an IPC standard. All test structures were subject to intermittent testing during their environmental exposure. This testing did not include electromigration analysis.

Each test article consisted of two silver barbell structures offset by 90° as shown in the corner of the top right plot in Figure 5. The two barbells are insulated from each other by a layer of polyimide at their intersection. This provided a portion of silver above and below the polyimide during the tests, simulating a multilayer circuit. The number of test articles per environment ranged from 112-192. Figure 5 shows the results of the three environmental tests. The resistance change over the duration of the test along with the number of failed modules is tracked. The error bars represent one standard deviation from the mean. As can be seen there is no noticeable change in resistance during the thermal shock testing, however there is over 42% module failure. This appears to be a result of adhesion degradation over the testing.

The moisture resistance test shows a significant change in standard deviation of the measurements but a less significant change in the mean resistance change. Module failure at the end of the test only reaches 7%. Similar to the thermal shock results, module failure appears to be primarily due to adhesion degradation between the conductor and the SiO2 substrate, a common failure mechanism for printed electronics.

Elevated temperature testing shows a significant mean resistance change but not an increase in measurement standard deviation nor any module failure. These test modules were sintered at 150°C for 1 hour, compared to 250°C for the IPC test articles. It can be inferred the mean resistance change is a direct consequence of sintering in the elevated temperature environment. Interestingly, when the structures are kept at a consistent temperature under lab humidity, the mean resistance variability is very low.

In conclusion, the AJP technology results in electronic systems fabrication with much greater versatility. Electrical resistance is 3-7X higher than bulk, which is acceptable for low frequency applications, but will result in an increase in parasitic power loss, which should be compensated for with trace design. For RF applications, the greatest challenge is improved control of dielectric thickness. Other challenges include electrical shorts resulting from layer-to-layer misalignment or conductive epoxy component attach. The work can be extended to a variety of substrates, inks and sintering methods.

The primary advantage of this method is concept-to-prototype fabrication time reduction from many weeks/months to days. Accelerated ageing shows generally good long term resistance performance, substrate adhesion as the primary failure mechanism, and that the inks could be useful in electronics applications for temperate environments. A SoC demonstration has been partially successful particularly for low frequency and digital domains, revealing challenges in adopting the technology for RF and IoT applications. Overall, AJP is a promising technology for rapid-prototyping of system interconnect.

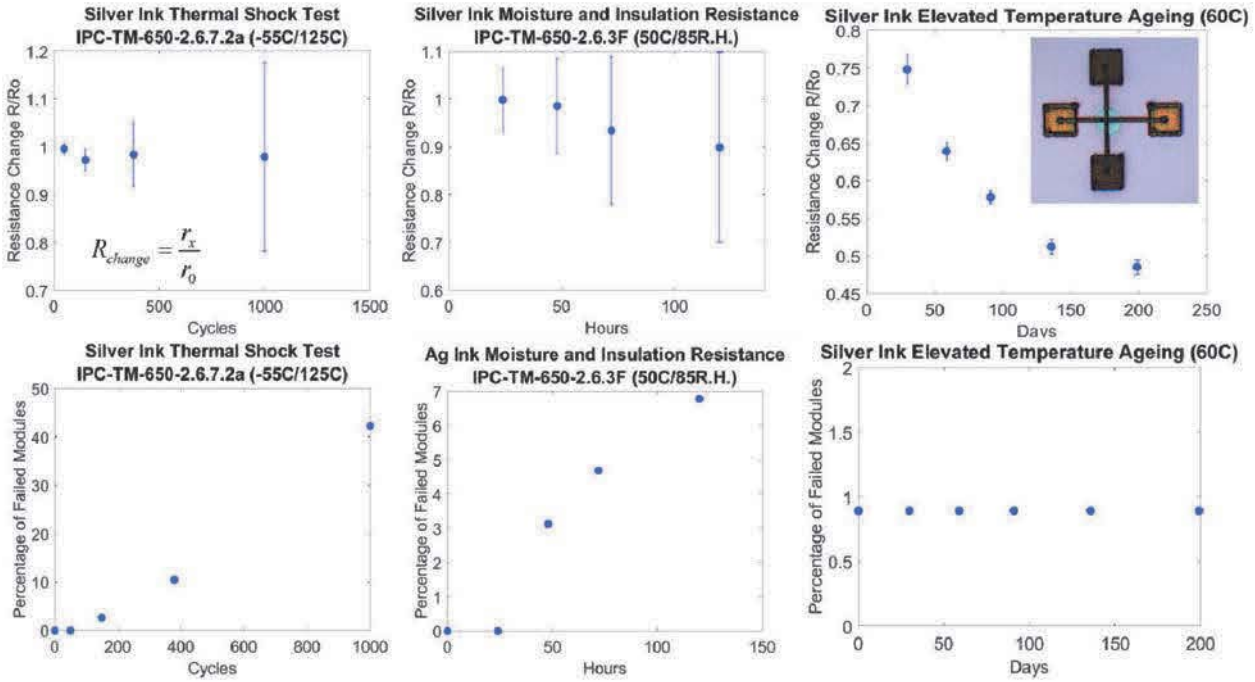

Figure 5: The accelerated ageing test results are shown above. Two tests were done to IPC standards while the third was done at elevated temperature in lab conditions. Each test included over a hundred structures with intermittent testing over the test. The testing occurred outside the environment. One structure is shown in the top right of the figure. The thermal shock results have a high module failure rate by the end of the testing, however the mean resistance change is fairly consistent. The moisture resistance test showed a much lower module failure rate and also a small change in mean resistance. The elevated temperature ageing shows virtually no module failure but a significant change in mean resistance. These modules were sintered at a lower temperature than the IPC test modules. A long term sintering of these modules is likely being observed.

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